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MICROELECTRONIC FABRICATION WITH UPPER LYING ALUMINUM FUSE
LAYER IN COPPER INTERCONNECT SEMICONDUCTOR TECHNOLOGY AND METHOD
FOR FABRICATION THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

001 The present invention relates generally to methods for fabricating microelectronic fabrications. More particularly, the present invention relates to methods for fabricating, with enhanced efficiency, microelectronic fabrications.

2. Description of the Related Art

002 Microelectronic fabrications are formed from microelectronic substrates over which are formed patterned microelectronic conductor layers which are separated by microelectronic dielectric layers.

003 As microelectronic fabrication integration levels have increased and microelectronic device and patterned microelectronic conductor layer dimensions have decreased, it has become increasingly common in the art of microelectronic fabrication, and in particular in the art of semiconductor integrated circuit microelectronic memory fabrication, to employ when fabricating microelectronic fabrications, and in particular when fabricating semiconductor integrated circuit microelectronic memory fabrications, fuse layers. Fuse layers in turn may be employed for purposes of severing from within a microelectronic fabrication non-functional portions of the microelectronic fabrication, such as but

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not limited to a block of non-functional memory cells within a semiconductor integrated circuit microelectronic memory fabrication, while providing for connection of redundant circuitry portions of the microelectronic fabrication, to provide an operational microelectronic fabrication from an otherwise non-operational microelectronic fabrication.

004 While fuse layers are thus clearly desirable in the art of microelectronic fabrication for fabricating microelectronic fabrications, and often unavoidable in the art of microelectronic fabrication for fabricating microelectronic fabrications, fuse layers are nonetheless not entirely without problems in the art of microelectronic fabrication for fabricating microelectronic fabrications.

005 In that regard, insofar as fuse layers within microelectronic fabrications are typically formed at earlier stages in fabrication of microelectronic fabrications, fuse layers often present difficulties in their access and actuation within microelectronic fabrications. Such difficulties in access and actuation of fuse layers is often particularly acute within an embedded memory semiconductor integrated circuit microelectronic memory fabrications where memory portions of the embedded memory semiconductor integrated circuit microelectronic memory fabrication are generally fabricated employing fewer conductor layers than logic portions within the embedded memory semiconductor integrated circuit microelectronic fabrication.

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006 It is thus desirable in the art of microelectronic fabrication to provide microelectronic fabrications, and methods for fabrication thereof, wherein fuse layers are more readily accessed and actuated.

007 It is towards the foregoing object that the present invention is directed.

008 Various microelectronic fabrications having formed therein fuse layers with desirable properties, and methods for fabrication thereof, have been disclosed in the art of microelectronic fabrication.

009 Included among the microelectronic fabrications and methods for fabrication thereof, but not limited among the microelectronic fabrications and methods for fabrication thereof are microelectronic fabrications and methods for fabrication thereof disclosed within: (1) Rodriguez et al., in U.S. Patent No. 5,821,160 (a semiconductor integrated circuit microelectronic memory fabrication, and method for fabrication thereof, which employ an etch stop layer for purposes of uniformly etching through a series of dielectric layers formed thereover within the semiconductor integrated circuit microelectronic fabrication without overetching into a fuse layer formed thereunder within the semiconductor integrated circuit microelectronic fabrication when etching through the series of dielectric layers and the etch stop layer within the semiconductor integrated circuit microelectronic

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fabrication to access and actuate the fuse layer within the semiconductor integrated circuit microelectronic fabrication); and (2) Hsiao et al., in U.S. Patent No. 5,985,765 (a microelectronic fabrication, and method for fabrication thereof, which employ a capping layer formed upon a bond pad layer such as to avoid over-etching into the bond pad layer when simultaneously etching within the microelectronic fabrication a comparatively shallow first via to access the bond pad layer within the microelectronic fabrication and a comparatively deep second via to access and actuate a fuse layer within the microelectronic fabrication).

0010 Desirable in the art of microelectronic fabrication, and particularly in the art of semiconductor integrated circuit microelectronic fabrication, and more particularly in the art of semiconductor integrated circuit microelectronic memory fabrication, are additional microelectronic fabrications, and methods for fabrication thereof, which provide for enhanced access and actuation of fuse layers within microelectronic fabrications.

0011 It is towards the foregoing object that the present invention is directed.

SUMMARY OF THE INVENTION

0012 A first object of the present invention is to provide a microelectronic fabrication, and a method for fabricating the microelectronic fabrication.

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invention may be fabricated employing methods and materials as are otherwise generally conventional in the art of microelectronic fabrication, but employed within the context of specific process limitations and specific structural limitations to provide a microelectronic fabrication in accord with the present invention. Since it is thus at least in part a series of process limitations and structural limitations which provides at least in part the present invention, rather than the existence of methods and materials which provides the present invention, the method of the present invention is readily commercially implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

0022 The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

0023 Fig. 1, Fig. 2, Fig. 3 and Fig. 4 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages of fabricating a microelectronic fabrication in accord with a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

0024 The present invention provides a microelectronic fabrication, and a method for fabricating the microelectronic fabrication, wherein there is provided for enhanced access and actuation of a fuse layer within the microelectronic fabrication.

0025 The present invention realizes the foregoing object by forming, when fabricating a microelectronic fabrication, a fuse layer at a level no lower than a highest of a series of patterned conductor layers within the microelectronic fabrication. By forming within the microelectronic fabrication in accord with the present invention the fuse layer at the level no lower than the highest of the series of patterned conductor layers within the microelectronic fabrication, the fuse layer is provided with enhanced access and actuation.

0026 Similarly, within the present invention the fuse layer is preferably formed of aluminum or an aluminum containing conductor material, while the series of patterned conductor layers is preferably formed of copper or a copper containing conductor material. Within the context of such materials selections, the fuse layer may be readily severed while employing standard fuse severing tooling.

0027 In addition, the present invention also preferably provides that the fuse layer is formed within a microelectronic fabrication simultaneously with at least one of a bond pad layer

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and an alignment mark layer, such that no additional masking process steps are required when forming the fuse layer in accord with the present invention.

0028 Although the present invention and the preferred embodiment of the present invention provide particular value within the context of fabricating an embedded memory semiconductor integrated circuit microelectronic memory fabrication, the present invention may be employed for fabricating, with enhanced access and actuation of fuse layers formed therein, microelectronic fabrications including but not limited to integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

0029 Referring now to Fig. 1 to Fig. 4, there is shown a series of schematic cross-sectional diagrams illustrating the results of progressive stages of fabricating a microelectronic fabrication in accord with a preferred embodiment of the present invention.

0030 Shown in Fig. 1 is a schematic cross-sectional diagram of the microelectronic fabrication at an early stage in its fabrication in accord with the preferred embodiment of the present invention.

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0031 Shown in Fig. 1, in a first instance, is a substrate 10 having formed thereover a first dielectric layer 12 which in turn has formed therein a series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e.

0032 Within the preferred embodiment of the present invention with respect to the substrate 10 (which provides a horizontal reference plane with respect to subsequent layers formed thereupon), and although, as noted above, the present invention provides particular value within the context of an embedded memory semiconductor integrated circuit microelectronic memory fabrication, the substrate 10, in addition to consisting of or comprising a semiconductor substrate as employed within a semiconductor integrated circuit microelectronic fabrication, may consist of or comprise a substrate as employed within a microelectronic fabrication selected from the group including but not limited to integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

0033 Although not specifically illustrated within the schematic cross-sectional diagram of Fig. 1, typically and preferably, but not exclusively, when the substrate 10 consists of or comprises a semiconductor substrate as employed within a semiconductor integrated circuit microelectronic fabrication, the

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substrate 10 has formed therein and/or thereupon microelectronic devices, and in particular semiconductor devices, as are conventional within the microelectronic fabrication within which is employed the substrate 10. Such microelectronic devices may be selected from the group including but not limited to resistors, transistors, diodes and capacitors.

0034 Within the preferred embodiment of the present invention with respect to the first dielectric layer 12, the first dielectric layer 12 may be formed from any of several dielectric materials as are otherwise generally conventional in the art of microelectronic fabrication, such dielectric materials being selected from the group including but not limited to conventional silicon containing dielectric materials (such as but not limited to silicon oxide dielectric materials, silicon nitride dielectric materials and silicon oxynitride dielectric materials), as well as lesser conventional low dielectric constant dielectric materials (such as but not limited to spin-on-glass (SOG) dielectric materials, spin-on-polymer (SOP) dielectric materials, amorphous carbon dielectric materials and fluorinated silicate glass (FSG) dielectric materials). Typically and preferably the dielectric layer 12 is formed as a laminate of from about 1 to about 8 dielectric sub-layers formed employing any of the foregoing dielectric materials, to form the dielectric layer 12 of thickness from about 100,000 to about 200,000 angstroms upon the substrate 10.

0035 Similarly, within the preferred embodiment of the present invention with respect to the series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e, the series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e may also be formed employing conductor materials as are generally conventional in the art of microelectronic fabrication, including but not limited to metal, metal alloy, doped polysilicon (having a dopant concentration of greater than about $1E18$ dopant atoms per cubic centimeters) and polycide (doped polysilicon/metal silicide stack) conductor materials, although within the preferred embodiment of the present invention, at least the upper portions of the series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e (and preferably all portions of the series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e) are formed of a copper or copper alloy (of copper content greater than about 90 weight percent) conductor material.

0036 Although also not specifically illustrated within the schematic cross-sectional diagram of Fig. 1, each of the series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e is intended to extend in an interconnected fashion completely through the first dielectric layer 12 such as ultimately to provide connection to a series of microelectronic devices formed within the substrate 10, particularly when the substrate 10 consists of or comprises a semiconductor substrate. Thus, similarly with the dielectric layer 12, the series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e is typically and preferably also formed

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of a series of patterned conductor sub-layers, generally comprising multiple series of patterned conductor interconnect sub-layers which are further interconnected with patterned conductor stud sub-layers, as is otherwise generally known in the art of microelectronic fabrication.

0037 In addition, and although also not specifically illustrated within the schematic cross-sectional diagram of Fig. 1, each of the patterned first conductor layers 14a, 14b, 14c, 14d and 14e typically and preferably has a linewidth of from about 2.0 to about 4.0 microns within the upper surface of the first dielectric layer 12.

0038 Further, and although also not specifically illustrated within the schematic cross-sectional diagram of Fig. 1, it is intended within the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1 that the patterned conductor layers 14b and 14c should be connected with a fuse and that the patterned conductor layer 14e should ultimately be connected to a bond pad.

0039 Finally, there is also shown within the schematic cross-sectional diagram of Fig. 1 formed upon the first dielectric layer 12 and the series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e a blanket passivation layer 16.

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0040 Within the preferred embodiment of the present invention, the blanket passivation layer 16 may be formed employing methods and materials as are conventional in the art of microelectronic fabrication. Typically and preferably, the blanket passivation layer 16 is formed to a thickness of from about 8,000 to about 12,000 angstroms from a silicon nitride passivation dielectric material or a silicon oxynitride passivation dielectric material.

0041 Referring now to Fig. 2, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1.

0042 Shown in Fig. 2 is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1, but wherein the blanket passivation layer 16 has been patterned to form a series of patterned passivation layers 16a, 16b, 16c and 16d which in turn define a series of apertures. Within the present invention, one of the apertures leaves exposed the pair of patterned first conductor layers 14b and 14c which are desired to be connected with the fuse, and another of the apertures leaves exposed the patterned first conductor layer 14e to which is desired to be formed the bond pad.

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0043 Within the preferred embodiment of the present invention, the blanket passivation layer 16 may be patterned to form the patterned passivation layers 16a, 16b, 16c and 16d while employing photolithographic patterning methods as are conventional in the art of microelectronic fabrication.

0044 Referring now to Fig. 3, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 2.

0045 Shown in Fig. 3 is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 2, but wherein there is formed upon exposed portions of the series of patterned passivation layers 16a, 16b, 16c and 16d, the first dielectric layer 12 and the series of patterned first conductor layers 14b, 14c and 14e a blanket aluminum containing conductor layer 18, although other conductor materials may also be employed.

0046 Within the preferred embodiment of the present invention, the blanket aluminum containing conductor layer 18 may be formed employing methods and aluminum containing conductor materials as are conventional in the art of microelectronic fabrication. Typically and preferably, the blanket aluminum containing conductor layer 18 is formed to a thickness of from about 1,000 to about

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16,000 angstroms from an aluminum conductor material or an aluminum containing conductor material of aluminum content of greater than about 99.5 weight percent.

0047 Referring now to Fig. 4, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 3.

0048 Shown in Fig. 4 is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 3, but wherein the blanket aluminum containing conductor layer 18 has been planarized to form a series of patterned planarized aluminum containing conductor layers 18a, 18b and 18c, wherein: (1) the patterned planarized aluminum containing conductor layer 18a forms an alignment mark; (2) the patterned planarized aluminum containing conductor layer 18b forms a fuse bridging the pair of patterned first conductor layers 14b and 14c; and (3) the patterned planarized aluminum containing conductor layer forms a bond pad contacting the patterned first conductor layer 14e. The alignment mark serves an alignment function with respect to the fuse and the bond pad.

0049 As is understood by a person skilled in the art, the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 6 may be electrically tested through

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electrical tester contact with the patterned planarized aluminum containing conductor layer 18c which forms the bond pad, and if needed the patterned planarized aluminum containing conductor layer 18b which forms the fuse layer may be actuated for purposes, for example, of severing within the microelectronic fabrication non-functional circuit elements. Thus, there is formed within the context of the present invention a microelectronic fabrication having formed therein a fuse layer which is readily accessed and actuated since the fuse layer is formed at a level within the microelectronic fabrication no lower than a highest of a series of patterned conductor layers (i.e., the series of patterned first conductor layers 14a, 14b, 14c, 14d and 14e) within the microelectronic fabrication, and preferably upon the highest of the series of patterned conductor layers within the microelectronic fabrication.

0050 As is further understood by a person skilled in the art, by employing within the context of the preferred embodiment of the present invention the series of patterned planarized aluminum containing conductor layers 18a, 18b and 18c which comprise the alignment mark, the fuse layer and the bond pad layer formed of an aluminum containing conductor material, each of those three layers is less susceptible to corrosion and oxidation which may impede the corresponding recognition, severing and bonding with respect to those three layers.

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0051 As is understood by a person skilled in the art, the preferred embodiment of the present invention is illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to methods, materials, structures and dimensions through which is fabricated a microelectronic fabrication in accord with the preferred embodiment of the present invention while still providing a microelectronic fabrication in accord with the present invention, and a method for fabrication thereof, further in accord with the accompanying claims.

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